

IEEE 802.3an LDPC Encoder/Decoder Core

Abstract

An optimized hardware efficient IEEE802.3an LDPC core (10Gbit/s Ethernet LDPC core) is presented. The proposed solution meets the performance requirements of the standard with outstanding power consumption and gate-count results.

I Introduction

Many applications have already positioned the new LDPC codes technology as a preferable ECC solution. The IEEE802.3an Task Force, for example, developing standard for 10Gbit/s Ethernet over twisted pair, unanimously adopted use of LDPC coding in August 2004.

We provide an Encoder/Decoder core which is specially tailored for the IEEE802.3an LDPC code. The core is based on a proprietary algorithmic solution and a proprietary decoder architecture, which provide a very efficient, high throughput, low complexity and low power solution.

II 10 Giga-Bit Ethernet (IEEE 802.3an)

10G bit Ethernet is part of the family of IEEE application standards developed for copper and fiber optic cabling that support 10 Gigabit per second (Gb/s) transmission rates. The published IEEE 802.3ae Standard is specified for fiber optic media and supports 10 Gb/s transmission rates for multiple fiber optic types. This new standard offers a straightforward upgrade path for Gigabit Ethernet backbones and makes provisions for linking Ethernet Local Area Networks (LANs) to Metropolitan and Wide Area Networks (MANs and WANs).

The recently published IEEE 802.3an standard describes the 10GBASE-T application for operation over category 6/class E (~50 meter), augmented category 6/class E, and class F twisted-pair copper cabling (~100 meter). The 802.3an was established to enable UTP-based solutions that are historically lower cost than their comparable fiber-based solutions. The 802.3an physical layer uses

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the existing 10 Gigabit Ethernet MAC and media independent interface as specified in IEEE 802.3ae™, 2002. It is intended that the IEEE 802.3an will provide very high rates of communication with low latency and IP driven Ethernet frame format, supporting the maximal and minimal frame lengths.

The physical layer of the 802.3an describes 4 unshielded twisted-pair connection per port utilizing the 500MHz bandwidth of the cable. Moreover, Near Shannon limit performance leverages multiple techniques, from pre-coding to a DSQ128 multi-level signaling. One of the most intriguing technologies is the Error Control Code, Low Density Parity Check (LDPC) maintaining BER of 10^{-13} . Together these techniques permit operation close to the Shannon limit. There are tradeoffs involved in achieving this goal, but power and latency are kept at acceptable levels.

The LDPC code is based on an algebraic construction, providing very low error floor ($< 10^{-13}$). It is (6,32)-regular RS-LDPC code of length 2048 and dimension 1723 [1]. The code's parity-check matrix used for decoding is a 6x32 block matrix constructed from 64x64 permutation blocks with redundant parity checks.

In the following sections we describe the developed highly-optimized, standard compliant, LDPC encoder /decoder core.

III Encoder hardware specification

The encoder supports the standard transmission rates with flexible wide range of clock frequencies starting from 1 MHz; the encoder produces the codeword within a low latency down to 30 ns. The gate-count for the encoder is ~27Kgates.

IV Decoder hardware specification

The high throughput required from the decoder and the specific structure of the IEEE802.3an LDPC code require unique solutions in order to facilitate an efficient high throughput, low complexity and low power decoder core. TurboBest's IEEE802.3an LDPC decoder core is based on a proprietary algorithmic solution accompanied by specially tailored decoder architecture for the IEEE802.3an LDPC code. These provide a very efficient, low complexity and low power decoder core supporting the required high throughput.

The decoder implementation supports streaming mode with coded bit rate of 6400 Mbits/sec. The decoder implements a fixed point version of Belief Propagation (BP) decoding algorithm, providing negligible performance loss compared to the floating point implementation (less than 0.1dB).

The decoder core supports statistical multiplexing that can be used for improving decoder performance at a given decoder clock rate on the expense of

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additional buffers and increased maximal decoding latency.

The decoder performance depends on the used decoder clock frequency and the amount of buffers used for statistical multiplexing. For example, Figure 1 shows fixed-point simulation results of the decoder, assuming no statistical multiplexing (i.e. no additional buffering and fixed decoding latency of 0.32 μ sec) at two decoder frequencies, 450 and 600 MHz.

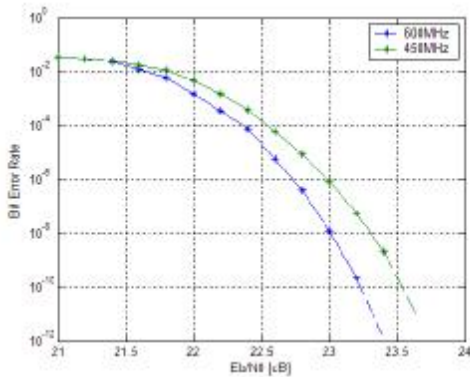


Figure 1 – fixed-point decoder simulation of the IEEE802.3an LDPC code, assuming fixed decoding latency of 0.32 μ sec at decoder clock frequencies of 450MHz and 600MHz.

V Decoder interface

The decoder pin-outs are defined in Table 1.

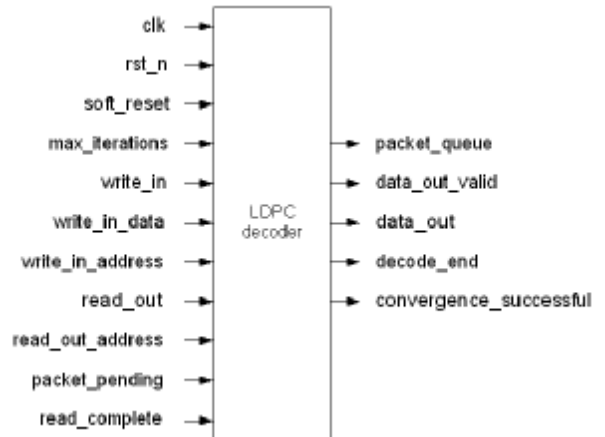


Figure 2 - Decoder block diagram

The decoder is supplied with two internal data buffers. Smart buffer management is designed to sustain high throughput in continuous decoding operation. Statistical multiplexing can be supported by managing additional buffering at the decoder's input.

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Signal name	Width	Direction	Details
clk	1	in	Decoder's clock.
rst_n	1	in	Asynchronous, active low reset.
soft_reset	1	in	Synchronous, active high reset. Optional reset to abort decoding and restart the decoder.
max_iterations	11	in	Set the number of clocks for packet decoding, each 48 clocks are 1 decoding iteration. This resolution enables better controllability for high throughput. This parameter is saved for each packet separately (with the "packet_pending" command)
write_in	1	in	Write enable of packet data into the decoder internal buffer.
write_in_data	1792	in	Packet data.
write_in_address	3	in	Buffer line address for the write operation.
read_out	1	in	Read command of the decoded data from decoder internal buffer.
read_out_address	3	in	Buffer line address for the read operation.
packet_pending	1	in	Command to the decoder. Indicate a new packet has been written into the decoder internal buffers.
read_complete	1	In	Host indication for end of reading of decoded data buffer.
packet_queue	2	out	Indicates the number of packets waiting for decoding inside the decoder.
data_out_valid	1	out	Indicates the output data is valid.
data_out	1792	out	Decoded data output.
decode_end	1	out	Indicates the decoder finished packet decoding.
convergence_successful	1	out	Indicates packet decoding has finished with 0 errors. If this signal is not asserted with "decode_end" it does not imply that the decoded packet contain errors.

Table 1 - Decoder Interface

References

[1] Amendment: Physical Layer and Management Parameters for 10 Gb/s Operation, Type 10GBASE-T, IEEE *Draft P802.3an/D2.1*

[2] I.Djurdjevic, J.Xu, K. Abdel-Ghaffar and S.Lin ",A Class of

LDPC Codes Constructed Based on Reed Solomon Codes With Two Information Symbols", IEEE Commun. Letters Vol 7, No 7, July 2003.